ECE 2610 Syllabus, Fall 2015

No: ECE 2610

Title: Digital Logic

Credits: 4 (LCT: 4)

WSU Catalog Description: Introduction to Boolean algebra, switches, gates, Minimization of switching circuits. ROMs, PROMs, and PLAs. Flip-Flops. Reduction and minimization of sequential machines. The state assignment problem. Asynchronous sequential circuits, Introduction to VLSI design.

Coordinator: Harpreet Singh, Professor of Electrical and Computer Engineering

Instructor: Harpreet Singh
Office Hours: 4:00 PM to 5:00 PM, T, TH
Office Location: 3111 Engg
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Course Meeting Time: 7:30 PM – 9:00 PM T-TH
Course Meeting Location: 1507 Engg

Goals: This course is designed to teach the basics of combinational and sequential logic circuits and design problems based on logic.

Learning Objectives: At the end of this course, students will be able to:

1. Illustrate the basics of Boolean algebra.
2. Explain techniques for minimization of Boolean functions
3. Design Simple Combinational circuits.
4. Design Simple sequential circuits.
5. Design ROM’s, PRAM’s and PLA’s
6. Introduction to FPGA’s and hardware description language


Prerequisites by Topic:

1. Number system

Co-requisites by Topic: None

Topics:

1. Boolean algebra and logic gates (1 week)
2. Simplification of Boolean functions (2 week)
3. Combinational logic (2 week)
4. MSI circuits like decoders, multiplexers, ROMs (2 week)
5. Sequential logic and state diagram reduction and assignment (2 week)
6. Design problems requiring flip-flops (2 week)
7. Asynchronous sequential circuits (2 week)
8. PLAs and memories. (1 week)

Course Structure: There are two 1 hour-50 min lectures per week. At the end of each lecture students goes to lab for half an hour.

Computer Resources: Desktops in the recently created FPGA LAB.

Laboratory Resources: FPGAs.

Laboratory Policy: There is absolutely no smoking: eating or drinking in any ECE instructional lab. These labs must be kept neat and each student is responsible for insuring that the equipment on his/her work bench is neatly arranged, that all the leads and other equipment are put away, and that there are no scraps of paper or other garbage left on or near his/her work station. Coats, briefcases: Knapsacks and other personal belongings are not permitted on or near the benches. These items must be kept on the coat rack near the door, not on the benches, window sills or the floor near the benches. The door to the lab must be kept locked at all times; unlocking or propping open the door at any time is expressly forbidden. Guests are not permitted in the lab at any time, and no one but the instructor may open the door to admit anyone after the class has begun.

Distribution of Points:

Test 1 20
Test 2 20
Final 25
Project 30
Home work 5

Grading Scale:

Lecture class grades: 75%
Lab class grades: 25%
Total Score: 100 %

Tentative subject to + or –5%

90-100 A
85 -89 A-
80-84 B+
75-79 B
70-74 B-
65-69 C+
Less than 50 F

- Each exam will have three questions
- Each question will have 32 points

4 points for bringing blue books and writing answers on inside cover page of blue book in Ink with your name

Attendance: You are expected to attend every lecture and lab session in its entirety. Do not schedule other classes or commitments that conflict with any part of the time during which your lab or lecture section is scheduled.

Homework:

Group Homework from Class Notes

Assignment 1 – tentative due at test 1 (*)

A1 – from notes

B1 – from text

Chapter 1: 1.1, 1.4, 1.8, 1.12, 1.16, 1.20

Chapter 2: 2.1, 2.3, 2.6, 2.8, 2.12, 2.14, 2.17, 2.21

Chapter 3: 3.1, 3.3, 3.5, 3.7, 3.16, 3.17, 3.23

Assignment 2 – tentative due at test 2 (*)

A2 – from notes

B2 – from text

Chapter 4: 4.1, 4.2, 4.8, 4.11, 4.22, 4.27
Chapter 5: 5.6, 5.10, 5.12, 5.20

Assignment 3 – tentative due by April 20 (*)

A3-1 and A3-2 – from notes

B3 – from text

Chapter 6: 6.17, 6.24, 6.27, 6.28

Chapter 7: 7.1, 7.8, 7.19, 7.22

(*) - you may submit only the part that was covered in class till time of submission

A1- Group HW from class notes

1. Write down a five variable truth table, for variables A, B, C, D and E.

2. Draw a Venn Diagram for \( f = A + AB + ABC \). What is this equal to? Prove this, using a truth table.

3. Assume you live 100 years. With three (3) candles, how many birthdays can you celebrate? Hint: Use different number systems.

4. Convert 37 (decimal) into base 2, 3, 4, 5, 6, 7 and 15.

5. Determine NOT of \( A + B + C \) on a Venn Diagram.

6. Determine NOT of \( ABC \).

7. Prove Question 5 using a truth table.

8. Prove Question 6 using a truth table as well.

A2- Group HW from class notes

1. Draw the BCD adder for page 130 of Mano Text Book, figure 4.14 at gate level by using any of the existing software.

   **Hint:** Use adders of figures 4.9 and 4.8. (i.e., use the 4-bit adder of fig, 4.9 in both adders of 4.14, and then use figure 4.8 to extend each of the full adders).

2. P 116 – Draw a BCD to Excess-3 Code converter using NAND gates

3. P119 – Incorporate 4 bit binary adder of Fig 4.9 in the BCD adder
4. P 134 – Draw a 2-4 decoder
5. Figure 4.21 – Incorporate 3-8 decoder of Fig 4.18
6. P 139 – Draw a 4-2 Encoder
7. P 142 – Draw a 2-1 multiplexer

**A3-1 - Homework Exercises**

1. Design SR flip-flop using T-flip-flop
2. Design SR flip-flop using JK flip-flop and T flip-flop using SR flip-flop
3. Design 1 and 2 using D flip flop
4. Design 1, 2 and 3 using computer aided method
5. Design a 0 through 7 Up-Counter using T flip-flop and computer aided method

**A3-2 - Homework Exercises**

1. Draw excitation table for D, T, S-R, J-K Flip Flops
2. P 199 – Draw the reduced State Diagram
3. P 263 - Draw memory cell using J-K Flip Flop
4. P 264 – Draw a 2-2 RAM and a 4-2 RAM
5. P 271 - Draw a ROM with k=2 and n=3
6. P 277 – Implement the following PLA

\[
F_1 (A,B,C) = \Sigma(0,1,2,6) \ F_2 \\
(A,B,C) = \Sigma(0,4,6,7)
\]

**FPGA Lab (Due at the time of Test 1)**

Attempt the Verilog design and simulation of:
- Examples 3.1, 3.2 and 3.3 from the Text Book.
Group project:

Prepare power point presentation of all the lecture notes. Modify the previous lecture notes. Submit it on a CD. Group presentation required during the last week of the classes.

**Verilog simulation and interpretation** of the results for all the Verilog examples up to chapter 6.

**Extra Credit**

To be announced.

**Schedule:**

**Tests**

Test 1 - First Thursday of October
Test 2 - First Thursday of November
Final Exam - According to schedule

- All tests open book open notes
- Project and homework by group of your choice
- Grades in project of all students in a group may not be same.

**Makeup Exam and Makeup Assignment Policy:** If a student thinks that he/she can’t take the exams on the scheduled dates due to some unavoidable circumstances, such as out of town, business trip, sickness, etc., then he/she must notify the instructor before the scheduled exam time. In that case the instructor may give a makeup exam to the student.

**Outcome Coverage:**

(a) *An ability to apply math, science and engineering knowledge.* The test requires direct application of mathematical, scientific, and engineering knowledge to successfully complete the course. This requires performing various linear digital design methods.

(b) *An ability to design and conduct experiments, as well as to analyze and interpret data.* Students conduct simple lab experiments using CD provided at the end of the text book.

(c) *An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.* The problems assigned require students to analyze and design simple digital circuits.

(e) *Identify, formulate and solve engineering problems.* The course is primarily oriented toward digital circuit design. The students design simple circuits and implement them using VERILOG in the lab and verify using FPGA implementation.
(h) The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context. The students are expected to learn the importance cost effective design so that designs require minimum number of gates and Flip Flops.

**Cheating Policy and Penalty for Cheating:** The students should not copy each other’s reports. During examination times no talking and passing papers or other items among the students will be allowed. The instructor will give an overall grade of F (Fail) to a student if that student is caught with any kind of cheating.

**Prepared By:** Harpreet Singh, Professor of Electrical and Computer Engineering

**Last Revised:** Aug. 28, 2015