ECE 3630 Syllabus, Fall 2006

No: ECE 3630

Title: Digital Circuits Laboratory

Credits: 2 (LCT: 1; LAB: 3)

WSU Catalog Description:
Prereq: or coreq: ECE 3610; coreq: MAT 2150. Design of decoders and other combinatorial logic circuits, design of flip-flops, counters, shift registers, and other sequential logic circuits. Choice of logic families, interfacing different logic families.

Coordinator: Dr. Harpreet Singh, Professor of Electrical and Computer Engineering

Instructor:
Bashar Qudah, Graduate Teaching Assistant of Electrical and Computer Engineering
Office: 3352 Engineering Building
Phone: (313) 577-1956
E-mail: bqudah@wayne.edu
Office Hour: 5:30 – 6:45 pm Monday
               2:00 – 3:15 pm Wednesday

Meeting Time: 12:50PM – 5:00PM Monday (September 5 – December 21, 2006)
Meeting Location: 1013 Industrial/Manufacturing Engineering Building

Goals: To develop competence in analysis, design, testing, and troubleshooting of simple digital circuits. To prepare students for more advanced courses in digital circuit analysis and design.

Learning Objectives: At the end of this course, students will be able to:
1. Measure digital circuit parameters using multimeters.
2. Verify the applications of transistor, inverter, decoder, counter and other combinational and sequential logic circuits by collecting and evaluating experimental data.
3. Construct various types of digital circuits to verify the applications of DeMorgan’s Theorem and Boolean Algebra
4. Analyze experimental data to verify various laws and theorems of digital circuits

Required Materials:
1. Digital Techniques Student Workbook, Heathkit Educational Systems
2. Digital Techniques Text Book, Heathkit Educational Systems


Prerequisites:
(ECE3310) Introduction to Boolean algebra; switches, gates. Minimization of switching circuits,
ROMs, PROMs, and PLAs. Flip-flops. Reduction and minimization of sequential machines. The state-assignment problem. Asynchronous sequential circuits.

Attendance Policy
You are required to attend the lab on time. The lab performance component of the grade will have a 10% overall weight for regular on time attendance. No lab make-up is allowed.

Lab Reports and Due Dates
An individual pre-lab one-page report is due at the beginning of each lab session. The report should cover the objectives of the experiments to be conducted during that lab session and a description of the functionality of the main new component(s) to be used in that lab session. Failure to submit a pre-lab report at the beginning of the lab session will result in a zero grade for that lab preparation.

An individual post-lab report is due by the beginning of the next lab session. The report should provide a detailed in depth discussion of the conducted experiment(s), answers selected questions and problems explicitly requested by the instructor, and highlight any problem or difficulty you ran through while implementing the experiment(s). The post-lab report should be 2 to 6 pages. Failure to submit a post-lab report at the beginning of the next lab session will result in a zero grade.

No late submission will be accepted. No lab report is accepted for a lab you did not attend. All reports should be typed and well organized. Submit the reports in hardcopy.

Exam and Quiz Policy
Examinations and quizzes are close books and notes. There will be a midterm, a final, and 2 short quizzes during this class. The quizzes are at the beginning of the class and the material they cover will be announced a week before. The midterm covers the material since the beginning up to the midterm day. The final covers the material since the midterm up to the final day. In case of unavoidable, documented emergency, which is reported in advance or immediately without delay when it becomes possible, a make-up exam (not quiz) maybe considered but not guaranteed. Otherwise the student will receive a zero for the missed exam or quiz.

Short Project
There will be a short project that you are required to design and to prepare for its implementation using the components you have in the lab kit. The project topic will be announced at least one week before its implementation date. The project should be implemented in full during the lab session reserved for that (as shown in schedule). The project can be done individually or in groups of 2 or 3 students. More details on the design, the implementation, and deliverables will be provided with the project announcement.

Laboratory Policy
There is absolutely no smoking, eating or drinking in any ECE instructional lab. These labs must be kept neat and each student is responsible for insuring that the equipment on his/her workbench is neatly arranged, that all the leads and other equipment be put away, and that there are no scraps of paper or other garbage left on or near his/her workstation.
Distribution of points

Lab On Time Attendance: 10%
Pre-Lab Reports & Preparation: 10%
In Lab Performance 10%
Post-Lab Reports: 20%
Short Project: 10%
Quizzes: 10%
Midterm Exam: 15%
Final Exam: 15%

Grading Scale

95 - 100 A
90 - 94 A-
85 - 89 B+
80 - 84 B
75 - 79 B-
70 - 74 C+
65 - 69 C
60 - 64 C-
50 - 59 D
0 - 49 F

Lab Schedule and Topics:

- Week 1 (9/11/06): Introduction to the Lab.
- Week 2 (9/18/06): Semiconductors Switches, and Inverters.
- Week 3 (9/25/06): Diode Logic, Transistor Logic Gates.
- Week 4 (10/2/06): TTL, CMOS Logic Gates.
- Week 5 (10/9/06): Quiz1, NAND and NOR Gates, Wired And Connections.
- Week 6 (10/16/06): S-R Flip Flop, D Flip Flop, J-K Flip Flop & Counters
- Week 7 (10/23/06): Mid Term Exam
- Week 8 (10/30/06): Binary Counters, BCD counter, Counter Applications
- Week 9 (11/6/06): Shift Register and Application
- Week 10 (11/13/06): Decoders, Multiplexers, 7-Segment Decoder-Driver and Display
- Week 11 (11/20/06): Quiz2, XOR/NOR, XOR /NOR applications
- Week 12 (11/27/06): Semiconductor Memories
- Week 13 (12/4/06): Short Project Implementation
- Week 14 (12/11/06): Final Exam

Cheating Policy and Penalty for Cheating

Academic Integrity: Academic dishonesty means any activity that tends to compromise the academic integrity of the institution or subvert the education process. All forms of academic dishonesty are prohibited at Wayne State University, as outlined in the Student Due Process Policy. Students are
expected to be honest and forthright in their academic studies. Students who commit or assist in committing dishonest acts are subject to downgrading and/or additional sanctions as described in the Student Due Process Policy. Faculty and students are responsible for knowing the different forms of academic dishonesty as well as for being aware of the Student Due Process Policy. It is important that each of us share the responsibility for maintaining a reputable University committed to academic excellence. Students should protect themselves by thoroughly studying and preparing for tests and assignments and by discouraging dishonesty among other students.

**Cheating:** Intentionally using or attempting to use, or intentionally providing or attempting to provide, unauthorized materials, information or assistance in any academic exercise. Examples: Copying from another student’s test paper. Allowing another student to copy from a test paper. Using unauthorized material such as a notebook during an exam.

**Fabrication:** Intentional and unauthorized falsification of any information or citation. Examples: Citation of information not taken from the source indicated. Listing sources in a bibliography not used in a research paper.

**Plagiarism:** To take and use another’s words or ideas as one’s own. Examples: Failure to use appropriate referencing when using the words or ideas of other persons. Altering the language, paraphrasing, omitting, rearranging, or forming new combinations of words in an attempt to make the thoughts of another appear as your own.

Other forms of academic dishonesty include, but are not limited to, the following acts: Examples: Unauthorized use of resources, or any attempt to limit another student’s access to educational resources, or any attempt to alter equipment so as to lead to an incorrect answer for subsequent users. Enlisting the assistance of a substitute in the taking of examinations. Violating course rules as defined in the course syllabus or other written information provided to the student. Selling, buying or stealing all or part of an un-administered test or answers to the test. Changing or altering a grade on a test or other academic grade records.

Any kind of cheating or violation of academic integrity is prohibited in this course. A STUDENT WHO CHEATS ON ANY ASSIGNMENT OR DURING ANY EXAM WILL BE ASSIGNED A FAILING GRADE FOR THIS COURSE.

**Outcome Coverage:**

(a) An ability to apply math, science and engineering knowledge. The homework and exams require direct application of mathematical, scientific, and engineering knowledge to successfully complete the course. This requires performing various linear circuit analysis methods in a formal manner and many supporting and follow-up calculations.

(b) An ability to design and conduct experiments, as well as to analyze and interpret data. Students conduct simple combinational and sequential digital circuit experiments.

(c) An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability. This outcome is a minor component of the course, but nevertheless present. A minority of the problems assigned requires students to calculate circuit parameter values (synthesis) rather than analyze circuit behavior. A few of the problems are multi-solution. Designs must be checked against real world operating limits such as saturation and power
limits.

(e) **Identify, formulate and solve engineering problems.** The course is primarily oriented toward digital circuit analysis and design but also includes examples of where digital circuit theory can be applied to other physical domains to model the system. Students must be able to identify the system, formulate a circuit model, and solve the circuit model to determine circuit variables, primarily with digital circuits.

(h) The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context. Students taking the course will realize the broad applicability of digital circuit analysis and design methods to electrical and other physical domains. "Topics in ECE" lectures provide a broad introduction to concepts, definitions and impact of different areas of electrical and computer engineering, including economic and social consequences of ECE innovations. Concept and definition questions are a small part of exams.

**Prepared By:** Bashar Qudah, Graduate Teaching Assistant of Electrical and Computer Engineering

**Last Revised:** September 6, 2006