ECE 5680 Syllabus, Winter 2012

No: ECE 5680

Title: Computer-Aided Logical Design and FPGAs Cr. 4 (LCT: 4)


Coordinator: Harpreet Singh, Professor of Electrical and Computer Engineering.
Instructor: Harpreet Singh, Professor of Electrical and Computer Engineering.
Office Hours: Office Location: 3111 Engineering Building
Phone: 313-577-3917
Email: hsingh@eng.wayne.edu
Web Page: http://ece.eng.wayne.edu/~singhweb

Course Meeting Time: Tue/Thr: 7:30-9:20pm
Course Meeting Location: 2409 Eng Bldg.

Goals: To teach how to design combinational circuits, sequential circuits and linear sequential circuits.

Learning Objectives: After completing this course, students should be able to do the following:

1. Illustrate the basics of Boolean algebra.
2. Explain techniques for minimization of large and multiple output boolean functions
3. Design of large Combinational circuits.
4. Design of large sequential circuits and linear sequential machines.
5. Design Boolean neural networks having large number of variables.
6. Illustrate basic concepts of binary descion diagrams
7. Illustrate basic concepts of VLSI Design


Reference Texts:
- N.N. Biswas, Introduction to Logic and Switching Theory
- N. Biswas, Logic Design Theory, Prentice Hall, 1993
- Handouts of several research papers.

Prerequisites by Topic: 1. Digital Logic Analysis
2. Combinational circuit design
Corequisites by Topic: none

Topics:

1. Review of Combinational and Sequential Circuits. (1 Week)

2. Selected Topics on Combinational Circuits. (1 Week)
   a) Gating functions for three or more variable cases (1 Week)
      - Minimization of combinational circuits for a very large number of variables.
      - Scheinman method for simplification of Boolean Functions
      - Scheinman method for overlapping and Non-overlapping cases
      - Scheinman method for multiple output simplification
      - Combination of Scheinman method and K-map method for
      - simplification of very large number of variables

   b) Boolean algebra applications in determining the Reliability of computer communication network. Scheinman Non-overlapping method for determining reliability. Fratta and Montanari method (F&M method) for determining terminal reliability. (1 Week)

   c) Boolean Algebra and Switching theory applications in the design of Computer circuits. Boolean algebra technique for designing pipelined arithmetic unit of a computer (1 Week)

   d) Special classes of combinational functions such as Unate functions and Threshold functions (1 Week)

   e) Design of threshold functions using Dertouzos method. (1 Week)
      - Design of Boolean functions using implied Minterm structure (IMS).
      - Design of Boolean functions using Minimal True and Maximal False vertices.
      - Use of K map in the design of Unate functions.
      - Correspondence between threshold gate and Neural networks.
      - Boolean neural network technique for target detections.

   f) Binary Decision Diagrams and their applications (1 Week)

   h) Fuzzy logic analysis and synthesis. (1 Week)
3. Selected topics on Sequential circuits.

a) T,R-S,J-K and their input equations. (1 Week)
   - Design of sequential circuits using D,T,R-S,J-K.
   - Computer aided design of sequential circuits using tabular charts for large number of variable cases

b) Reduction of sequential circuits and design using various flip flops. Huffman Mealy procedure for reduction of sequential circuits. (1 Week)

c) Design of linear sequential machines using unit delays, modulo p adders and modulo p scalar multipliers. (1 Week)

d) Reduction of linear machines. Diagnostic matrix, Minimization procedure and realization of reduced machines. (1 Week)

e) Identification of linear machines. Identification procedure, Use of distinguishing tables in the design of linear sequential machines. (1 Week)

Course Structure: There are two 1 hour 50 mins Lectures per week. At the end of each lecture students will go to VLSI Lab and UNIX lab for half an hour.

Computer Resources: Students will be using Unix Work Stations on different VLSI CAD tools like L-EDIT and CADENCE in recently created VLSI Lab and FPGA Lab.

Laboratory Resources: A laboratory containing 9 PCs, several high-end multimeters, function generators and oscilloscopes is available for the students.

Laboratory Policy: There is absolutely no smoking: eating or drinking in any ECE instructional lab. These labs must be kept neat and each student is responsible for insuring that the equipment on his/her workbench is neatly arranged, that all the leads and other equipment are put away, and that there are no scraps of paper or other garbage left on or near his/her work station. Coats, briefcases: Knapsacks and other personal belongings are not permitted on or near the benches. These items must be kept on the coat rack near the door, not on the benches, window sills or the floor near the benches. The door to the lab must be kept locked at all times; unlocking or propping open the door at any time is expressly forbidden. Guests are not permitted in the lab at any time, and no one but the instructor may open the door to admit anyone after the class has begun.

Project: The project report must contain the following items in the same order as shown below.

The project consists of VLSI implementation of exclusive OR, full adder. They should have capability so that the design can be sent to MOSIS. The students are also expected to give group presentation on one research paper.

Distribution of Points:
Grading Scale: Percentage Grade (tentative subject to + or –5%)

<table>
<thead>
<tr>
<th>Percentage Range</th>
<th>Grade</th>
<th>GPA</th>
</tr>
</thead>
<tbody>
<tr>
<td>90-100</td>
<td>A</td>
<td>4.00</td>
</tr>
<tr>
<td>85-89</td>
<td>A-</td>
<td>3.67</td>
</tr>
<tr>
<td>80-84</td>
<td>B+</td>
<td>3.33</td>
</tr>
<tr>
<td>75-79</td>
<td>B</td>
<td>3.00</td>
</tr>
<tr>
<td>70-74</td>
<td>B-</td>
<td>2.67</td>
</tr>
<tr>
<td>65-69</td>
<td>C+</td>
<td>2.33</td>
</tr>
<tr>
<td>60-64</td>
<td>C</td>
<td>1.67</td>
</tr>
<tr>
<td>55-59</td>
<td>C-</td>
<td>1.67</td>
</tr>
<tr>
<td>50-54</td>
<td>D+</td>
<td>1.33</td>
</tr>
<tr>
<td>Less than 50</td>
<td>F</td>
<td></td>
</tr>
</tbody>
</table>

- Each exam will have three questions
- Each question will have 32 points
- 4 points for bringing blue books and writing answers on inside cover page of blue book in Ink with your name

Attendance: Every student is expected to attend all lectures. All students must also attend their regular group meetings.

Schedule:

1. Test1: 1st week of February, 2012
2. Test2: 1st week of March, 2012
3. Final: according to the university schedule.

Makeup Exam and Makeup Assignment Policy:

- All assignments must be submitted on time. No late submission will be accepted unless the student notifies the instructor ahead of time showing some valid reasons (such as town of out business trip, sickness, etc.) for not being able to submit the assignment on time. The student must present valid official documents to defend his/her case.
- All students must take the midterm on the scheduled date. If a student thinks that he/she can't take the midterm on the scheduled date due to some unavoidable circumstances, such as out of town business trip, sickness, etc., then he/she must notify the instructor before the scheduled exam time. In that case the instructor may give a makeup exam to the student. However, the student must present valid official documents to defend his/her case.

Outcome Coverage:

(a) An ability to apply math, science and engineering knowledge. The test requires direct application of mathematical, scientific, and engineering knowledge to successfully complete the course. This requires performing various linear digital design of combinational and sequential circuits, Design of Boolean neural networks and fuzzy logic circuits.
(b) An ability to design and conduct experiments, as well as to analyze and interpret data. Students conduct simple lab experiments in VLSI in UNIX lab using VERILOG.

(c) An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability. The problems assigned require students to analyze and design simple digital circuits, Boolean neural nets and fuzzy logic circuits.

(e) Identify, formulate and solve engineering problems. The course is primarily oriented toward digital circuit design. The students design simple circuits and implement them using VERILOG in the lab and verify using FPGA implementation.

(h) The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context. The students are expected to learn the importance cost effective design so that designs require minimum number of gates and Flip Flops. The students are expected to design second generation of Boolean logic circuits having large number a variables.

**Cheating Policy and Penalty for Cheating:** The students should not copy each others reports. During examination times no talking and passing papers or other items among the students will be allowed. The instructor will give an overall grade of F (Fail) to a student if that student is caught with any kind of cheating.

**Prepared By:** Harpreet Singh, Professor of Electrical and Computer Engineering

**Last Revised:** January 1st, 2012