EET 3100
Advanced Digital Design

Instructor: Moise Sunda

Office Hours: Before Class / By Appointment

Telephone: 586-212-4431

Email: ag6642@wayne.edu
       msunda@wayne.edu

Course Details:
Course: Advcd Digitl Desgn - EET 3100 – Sec: 901 – CRN: 26646
Location: ATEC (Advanced Technology Education Center) – Room 150
         14601 E. 12 Mile Road
         Warren, MI 48088
Day/Time: Tuesdays 5:30pm – 8:00pm

Course Description:
System level design of digital logic circuits using hardwired and programmable logic
devices. ROMs, PROMs, and PLAs. Synchronous and asynchronous circuit design and
analysis.

Credit Hours:
3  (Lct: 2, Lab: 2)

Prerequisite:
EET 2100 Principles of Digital Design

Text(s) (Recommended):
Publishing. ISBN: 140184030-2 or 9781401840303

Computer Programs:
Quartus II v9.1 SP2 will be used.
You can download the free version from www.altera.com

Course Contents:
Karnaugh Map Review
Combinational Circuit Design
   Adder/Subtractor
   Comparators
   Parity Generators and Checkers
   Design with Decoders/Multiplexers
Synchronous Sequential Circuit Design
   State Machine Design
   Analysis of Clocked Sequential Circuits
   State Reduction and Assignment
   Counter Design
   Shift Register Design
Memory Devices and Systems
Programmable Logic Devices (PLD)
   Programmable Read Only Memory (PROM)
   Programmable Logic Array (PLA)
   Programmable Array Logic (PAL)
Asynchronous Sequential Design

Laboratory:
The laboratory consists of hands-on and simulation assignments that will accompany the lectures of EET 3100. The goal is to illustrate the concepts discussed in class and to give students the opportunity to build and test real systems. Students are required to work individually for each assignment and submit individual laboratory reports. There are two hardware laboratory assignments where group work is required. For these laboratories, you will work in groups of two and submit only one laboratory report for the group. There will be a formal team member assessment form that each of you will fill out.

The lab exercises will make use of the Altera Design System, which is a powerful state-of-the-art tool for designing and implementing digital systems using Complex Programmable Logic Devices (CPLD). CPLDs can be programmed, erased, and reprogrammed via a connection to a PC’s serial port, parallel port, or USB connection. You can download the free student version from www.altera.com website. Please refer to the laboratory syllabus for further information.

ABET (Accreditation Board for Engineering and Technology)

Program Educational Objectives – Program educational objectives are broad statements that describe what graduates are expected to attain within a few years of graduation. Program educational objectives are based on the needs of the program’s constituencies.

BS-EET Program Educational Objectives:
The main objective of the Bachelor of Science in Electrical/Electronic Engineering Technology (BS-EET) Program is to provide an outstanding curriculum and learning environment, so that, following completion of the program, BSET-EET graduates will be able to:
   • attain gainful employment and practice successfully in an electrical or electronic related engineering technology profession;
• remain technically current and adapt to rapidly changing technologies through continuous learning and self-improvement;
• demonstrate independent thinking and function effectively in teams to solve open-ended problems in an industrial environment;
• communicate effectively and perform ethically and professionally in business, industry, and society.

Student Outcomes – Student outcomes describe what students are expected to know and be able to do by the time of graduation. These relate to the skills, knowledge, and behaviors that students attain as they progress through the program.

### ABET Criterion 3. Student Outcomes

An engineering technology program must demonstrate that graduates have:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>a.</td>
<td>an ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities;</td>
</tr>
<tr>
<td>b.</td>
<td>an ability to select and apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require the application of principles and applied procedures or methodologies;</td>
</tr>
<tr>
<td>c.</td>
<td>an ability to conduct standard tests and measurements; to conduct, analyze, and interpret experiments; and to apply experimental results to improve processes;</td>
</tr>
<tr>
<td>d.</td>
<td>an ability to design systems, components, or processes for broadly-defined engineering technology problems appropriate to program educational objectives;</td>
</tr>
<tr>
<td>e.</td>
<td>an ability to function effectively as a member or leader on a technical team;</td>
</tr>
<tr>
<td>f.</td>
<td>an ability to identify, analyze, and solve broadly-defined engineering technology problems;</td>
</tr>
<tr>
<td>g.</td>
<td>an ability to apply written, oral, and graphical communication in both technical and non-technical environments; and an ability to identify and use appropriate technical literature;</td>
</tr>
<tr>
<td>h.</td>
<td>an understanding of the need for and an ability to engage in self-directed continuing professional development;</td>
</tr>
<tr>
<td>i.</td>
<td>an understanding of and a commitment to address professional and ethical responsibilities including a respect for diversity;</td>
</tr>
<tr>
<td>j.</td>
<td>a knowledge of the impact of engineering technology solutions in a societal and global context; and</td>
</tr>
<tr>
<td>k.</td>
<td>a commitment to quality, timeliness, and continuous improvement.</td>
</tr>
</tbody>
</table>

### ABET EET Program Criteria

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>E1</td>
<td>the ability to analyze, design, and implement control systems, instrumentation systems, communications systems, computer systems, or power systems.</td>
</tr>
<tr>
<td>E2</td>
<td>the ability to apply project management techniques to electrical/electronic(s) systems.</td>
</tr>
<tr>
<td>E3</td>
<td>the ability to utilize statistics/probability, transform methods, discrete mathematics, or applied differential equations in support of electrical/electronic(s) systems.</td>
</tr>
<tr>
<td>E4</td>
<td>the ability to apply circuit analysis and design, computer programming, associated software, analog and digital electronics, and microcomputers, and engineering standards to the building, testing, operation, and maintenance of electrical/electronic(s) systems.</td>
</tr>
<tr>
<td>E5</td>
<td>the ability to apply physics or chemistry to electrical/electronic(s) circuits in a rigorous mathematical environment at or above the level of algebra and trigonometry.</td>
</tr>
</tbody>
</table>
EET3100 Course Learning Objectives

<table>
<thead>
<tr>
<th></th>
<th>Program Outcomes</th>
<th>Assessment Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>a,b</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>a,b,c,d,f,E1, E4</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>a,b,c,d,f,E1, E4</td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>a,b,c,d,f,E1, E4</td>
<td></td>
</tr>
<tr>
<td>5.</td>
<td>a,b,c,f,E1, E4</td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>a,b,c,f,E1, E4</td>
<td></td>
</tr>
<tr>
<td>7.</td>
<td>a,b,c,f,E1, E4</td>
<td></td>
</tr>
<tr>
<td>8.</td>
<td>a,E1, E4</td>
<td>Lab</td>
</tr>
<tr>
<td>9.</td>
<td>a,E1, E4</td>
<td>Lab</td>
</tr>
<tr>
<td>10.</td>
<td>a,E1, E4</td>
<td>Lab</td>
</tr>
<tr>
<td>11.</td>
<td>a,b,c,d,f,E1, E4</td>
<td></td>
</tr>
<tr>
<td>12.</td>
<td>a,b,c,d,f, E4</td>
<td></td>
</tr>
<tr>
<td>13.</td>
<td>c,k, E4</td>
<td>Lab</td>
</tr>
<tr>
<td>14.</td>
<td>e,i,k, E4</td>
<td>Lab</td>
</tr>
</tbody>
</table>

**Assessment:**
Exams (2): 20% each
Final Exam: 25%
Labs: 25%
Homework: 10%

A grade of "I" will only be assigned if a student IS NOT currently failing the course and if there is NOT a substantial amount of work to be completed. An “I” grade MUST be made up within one year of the assignment of the grade. The assignment of an “I” grade will be at the sole discretion of the instructor.

**Grading Scale:**

A 93-100
A- 90-92
B+ 87-89
B  83-86
B- 80-82
C+ 77-79
C  73-76
C- 70-72
D+ 67-69
D  63-66
D- 60-62
E  Below 60

Class Policies:
- Each exam date will be announced in class (and via Blackboard) at least two weeks before the exam date.
- Attendance for tests and the final exam is mandatory. Make-up exams will not be given. See the professor ASAP if there is a conflict with a test or the final exam.
- No formal class attendance will be taken. The course content follows lecture notes closely and a student’s success will generally be directly related to the class attendance.
- Using or attempting to use unauthorized assistance or material will result in a zero grade for the course.
- Blackboard will be used throughout the course for communication among students and with the instructor. You will find all assignments, exam dates, solutions, study guides, etc on the Blackboard site. You can also check your grades online.
- Activate your Wayne State email address. This will be the email address with which I will communicate with the class.
- Homework and Laboratory assignments will be posted on Blackboard.
  - Due dates for assignments will be posted and are expected to be on time.
  - Late homework assignments or laboratory reports will NOT be accepted.
  - All assignments must be submitted electronically via Blackboard.
  - All assignments must be in Microsoft Word format using features available in MS Word or Excel.
  - Handwritten assignments will not be accepted (this includes scans and/or photos of handwritten assignments).
  - It is your responsibility that you submit the correct document under the correct assignment. After you submit your assignment, click on the document to make sure it is correct.
  - The following naming convention must be used for your submissions. Failure to do so will result in points being deducted from your assignment.

    assignment_Last nameFirst initial.docx

    Examples:
    HW1_SundaM.docx
    Lab1_SundaM.docx

University / Department Policies:
Academic Integrity
http://doso.wayne.edu/academic-integrity.html
Cheating includes but is not limited to GIVING or RECEIVING unauthorized help on an examination. Cheating includes the use of unauthorized material during an examination or submitting material on the lab reports or course projects which is not the result of the student’s own effort. Cheating also includes plagiarism – avoid even grey areas of plagiarism.

**Students with Disabilities:**
http://studentdisability.wayne.edu/accommodations.php
If you have a documented disability that requires accommodations, you will need to register with Student Disability Services (SDS) for coordination of your academic accommodations. The Student Disability Services (SDS) office is located at 1600 David Adamany Undergraduate Library in the Student Academic Success Services department. SDS telephone number is 313-577-1851 or 313-577-3365 (TDD only). Once you have your accommodations in place, the instructor will meet with you privately to discuss your special needs. Student Disability Services’ mission is to assist the university in creating an accessible community where students with disabilities have an equal opportunity to fully participate in their educational experience at Wayne State University. Please be aware that a delay in getting SDS accommodation letters for the current semester may hinder the availability or facilitation of those accommodations in a timely manner. Therefore, it is in your best interest to get your accommodation letters as early in the semester as possible.

**School Closure**
School closing are posted to Wayne State’s main web page http://www.wayne.edu/. You can also setup notifications thru Pipeline to be notified in the event of school closure by email or text.

**Code of Ethics for Engineers:**


http://www.ieee.org/about/corporate/governance/p7-8.html

**Moise Sunda** (updated: March 21, 2017)