ECE 6660 Syllabus, Fall 2011

No: ECE 6660

Title: Introduction to VLSI Systems. Cr. 4 (LCT: 4)

WSU Catalog Description:

Prereq: ECE 4680, ECE 5680 or consent of instructor. Digital systems and VLSI, Transistors and layout, Logic gates, Combination Logic, Networks, Sequential machines, Subsystem design, Floor Planning, Architecture, Design, Chip Design, CAD Systems and Algorithms, Survey of very large scale integrated circuit components and design procedures. MOS fabrication, MOS gates, circuit architecture device design, manufacturing and interface techniques.

Coordinator: Harpreet Singh, Professor of Electrical and Computer Engineering

Instructor: Harpreet Singh

Office Hours: 3:00-4:00 PM Mon & Wed


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Course Meeting Time: 7:30 to 9:20 Mon & Wed

Course Meeting Location: 2409, Engg. Bldg.

Goals: This course is designed to give introductory concepts of VLSI and systems approach to the design of VLSI systems.


Reference Books:

- Introductory VHDL from Simulation to synthesis by Sudhakar Yalamanchili, Xilinx Design Series
- Advanced Digital Design with the VERILOG HDL by Michael D. Ciletti, Xilinx Design Series
- Introduction to VLSI Systems by Carver Mead, Lynn Conway, Addison-Wesley Publishing Company
Learning Objectives: After completing this course, students should be able to do the following:

1. Illustrate the basics of VLSI design.
2. Design digital circuits using Verilog.
3. Illustrate the steps to send the design to MOSIS.
4. Develop the VLSI implementation of combinatorial circuits.
5. Develop the VLSI implementation of sequential circuits.
6. Identify constraints for system design approach for VLSI implementation.

Prerequisites by Topic: ECE 4680 and ECE 5680

1. Switching theory
2. Computer Architecture
3. Computer Design

Topics:

1. Digital systems and VLSI, CMOS technology, integrated circuit design techniques. (1 Week)
2. Transistors and layout, Design rules, layout design and tools. (1 Week)
3. Logic gates, combinational logic functions, switch logic, alternative gate circuits, delay through interconnects. (2 Week)
4. Combination Logic Networks, fan-out, wire sizing, gate testing, combinational network testing. (2 Week)

5. Sequential machines, latches and flip flops, one phase and two phase systems, power optimization. (2 Week)

6. Subsystem design, pipelining, data-paths, headers, ALU’s, multipliers, field-programming gate arrays, PLA’s. (2 Week)

7. Floor Planning, Global routing, design validation, Pad design. (1 Week)

8. Architecture, Design, VERILOG, register transfer design. (1 Week)

9. Chip Design, Design methodologies, logic and layout design, data path organization. (1 Week)

10. CAD Systems and Algorithms, layout synthesis, hardware software co-design. (1 Week)

**Course Structure:** There are two 1 hour 50 mins Lectures per week. At the end of each lecture students will go to VLSI Lab and UNIX lab for half an hour.

**Computer Resources:** Students will be using Unix Work Stations on different VLSI CAD tools like L-EDIT and CADENCE in recently created VLSI Lab.

**Laboratory Policy:** There is absolutely no smoking: eating or drinking in any ECE instructional lab. These labs must be kept neat and each student is responsible for insuring that the equipment on his/her work bench is neatly arranged, that all the leads and other equipment are put away, and that there are no scraps of paper or other garbage left on or near his/her work station. Coats, briefcases: Knapsacks and other personal belongings are not permitted on or near the benches. These items must be kept on the coat rack near the door, not on the benches, window sills or the floor near the benches. The door to the lab must be kept locked at all times; unlocking or propping open the door at any time is expressly forbidden. Guests are not permitted in the lab at any time, and no one but the instructor may open the door to admit anyone after the class has begun.

**Distribution of Points: Suggested:**

**Grading Scale:**

- Test 1: 20
- Test 2: 20
- Final: 25
- Project: 30
- Home work: 5

**Grading** tentative subject to + or –5%
90-100     A
85 -89      A-
80-84       B+
75-79       B
70-74       B-
65-69       C+
60-64       C
55-59       C-
50-54       D+
Less than 50 F

- Each exam will have three questions
- Each question will have 32 points
- 4 points for bringing blue books and writing answers on inside cover page of blue book in Ink with your name

Schedule:

Tests:
1. Test1: Wednesday, October 5, 2011
2. Test2: Wednesday, November 2, 2011
3. Final: Wednesday, December 14, 2011

Homework: The student are expected to do home work problems given to them from time to time.

Project: The project consists of VLSI implementation of exclusive OR, full adder and generalized pipeline array circuits. They should have capability so that the design can be sent to MOSIS. The students are also expected to give group presentation on one research paper.

Makeup Exam and Makeup Assignment Policy: Assignment Policy: If a student thinks that he/she can’t take the exams on the scheduled dates due to some unavoidable circumstances, such as out of town, business trip, sickness, etc., then he/she must notify the instructor before the scheduled exam time. In that case the instructor may give a makeup exam to the student.

Outcome Coverage:
(a) An ability to apply math, science and engineering knowledge. The assignments, tests, exam and project require direct application of mathematical, scientific, and engineering knowledge to successfully complete the course. This requires introductory VLSI design concepts.

(b) An ability to design and conduct experiments, as well as to analyze and interpret data. A major focus of the course is to teach students how to design VLSI gates, combinational and sequential circuits. The students are expected to do exercises using VERILOG language.

(c) An ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability. Students work in teams of four students. The assignments involve the design of various VLSI concepts.

(d) An ability to function on multi-disciplinary teams: Students work or their design assignments and projects in teams of four students. The project work involves the design of electronic controllers, automated vehicles, voice activated devices and many other types of systems that are of multi-disciplinary types. Organization and active contribution to team effort is required in the course.

(e) Identify, formulate and solve engineering problems. The students achieve this item as they analyze a given problem in VERILOG language.

(g) An ability to communicate effectively: All students are required to make an group oral presentation on their project work. The students are also required to submit a well-written technical report on their project work. The oral presentation and technical report writing process help them in achieving effective communication skills.

(k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice: Students learn to use the VERILOG, L Edit software and cadence software, a modern tool developed by Microchip. Students also use the latest state-of-the-art sensors, actuators, analog and digital integrated chips, and other components for the assignments and project work.

**Cheating Policy and Penalty for Cheating:** The students should not copy each others reports. During examination times no talking and passing papers or other items among the students will be allowed. The instructor will give an overall grade of F (Fail) to a student if that student is caught with any kind of cheating.

**Prepared By:** Harpreet Singh, Professor of Electrical and Computer Engineering

**Last Revised:** October 31, 2011